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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,063	HARER ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/12/01 & 2/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 were reviewed for prosecution.

Abstract

2. The acronym, DUT, should be spelled out.

Trademarks

3. The use of trademarks for UNIX™, C/C++™, Pascal™ and CorerBooster™ have not been properly noted in the specification (e.g., pg. 32, line 5;and pg. 37, line 2). The trademark notation should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner, which might adversely affect their validity as trademarks.

Appendix

4. Appendices I and II have computer code of more than 300 lines. In accordance with 37 CFR 1.96(c), a computer program listing contained on more than three hundred (300) lines, must be submitted as a computer program listing appendix on compact disc conforming to the standards set forth in 37 CFR 1.96(c)(2) and must be appropriately referenced in the specification (see 37 CFR 1.77(b)(4)). Accordingly, applicant is required to cancel the computer program listing appearing in the current appendix to the specification, file a computer program listing appendix on compact disc in compliance

with 37 CFR 1.96(c), and insert an appropriate reference to the newly added computer program listing appendix on compact disc at the beginning of the specification.
A computer program listing on compact disc filed with a patent application will be referred to as a Computer Program Listing Appendix on compact disc and will be identified as such on the front page of the patent but will not be part of the printed patent. "Computer Program Listing Appendix on compact disc" denotes the total computer program listing files contained on all compact discs. The face of the file wrapper will bear a label to denote that an appendix on compact disc is included in the application. A statement must be included in the specification to the effect that a computer program-listing appendix on compact disc is included in the application. The specification entry must appear at the beginning of the specification immediately following any cross-reference to related applications. *37 CFR 1.77 (b)(4).* The patent front page and the Official Gazette entry will both contain information as to the names and sizes of files on compact discs of computer program listings appearing in the computer program-listing appendix on compact disc. When an application containing compact discs is received in the Office of Initial Patent Examination (OIPE), a special envelope will be affixed to the right side of the file wrapper underneath all papers, and the compact discs inserted therein. The application file will then proceed on its normal course.

Information Disclosure Statement

5. The listing of references in the specification (e.g., page 14, lines 13-19; page 15, lines 1-5, page 23, lines 8-10; page 31, lines 6-9) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other

information submitted for consideration by the Office, and MPEP § 609 A (1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Interpretation

6. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. **The examiner interprets formal simulation as symbolic simulation; and the interleaving or combination of symbolic and formal to be same for one particular test /execution.**

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to using two types of simulation microprocessors. The examiner respectfully submits that the applicants have not claimed a practical application. An invention which is eligible for patenting under 35 U.S.C. § 101 is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The fundamental test for patent eligibility is thus to determine whether the claimed invention produces a "useful, concrete and tangible result." The test for practical application as applied by the examiner involves the determination of the following factors:

> (1) "Useful" - The Supreme Court in *Diamond v. Diehr* requires that the examiner look at the claimed invention as a whole and compare any asserted utility with the claimed invention to determine whether the asserted utility is accomplished. Applying utility case law the examiner will note that:
>
> > (a) the utility need not be expressly recited in the claims, rather it may be inferred.
> > (b) if the utility is not asserted in the written description, then it must be well established.
>
> (2) "Tangible" - Applying *In re Warmerdam*, 33 F.3d 1354, 31 USPQ2d 1754 (Fed. Cir. 1994), the examiner will determine whether there is simply a mathematical construct claimed, such as a disembodied data structure and method of making it. If so, the claim involves no more than a manipulation of an abstract idea and therefore, is nonstatutory under 35 U.S.C. § 101. In *Warmerdam* the abstract idea of a data structure became capable of producing a useful result when it was fixed in a tangible medium, which enabled its functionality to be realized.
>
> (3) "Concrete" - Another consideration is whether the invention produces a "concrete" result. Usually, this question arises when a result cannot be assured. An appropriate rejection under 35 U.S.C. § 101 should be accompanied by a lack of enablement rejection, because the invention cannot operate as intended without undue experimentation.

The examiner respectfully submits, under current PTO practice, that the claimed invention does not recite a tangible or concrete result. The claims are not tangible because they appear to recite a mathematical algorithm in a limited space that doesn't have specific preprocessing or post solution activity.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1-36 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The specification does not clearly define "a goal state", "progress metric" and "previously-defined goal states"; or their criteria.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

12. The following claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

- Claims 1-35: progress metric—ambiguous.

- Claims 4,5, 12, 13, 20, 21,28,29: satisfiability technique—vague and indefinite.
- Claims 7, 15, 23, 32: previously-defined sets and unreachable—vague and ambiguous.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

14. Claims 1-5, 9-13,17-21,25-29 are rejected under 35 U.S.C. 102 (a) as being anticipated by Ho et al. ("Smart Simulation Using Collaborative Formal and Simulation Engines"; IEEE (November 2000)).

Ho et al. teaches a simulation-based functional verification tool which provides automatic test generation and unreachability analysis (abstract: lines 1-5).

Claim 1: A method of verifying a design for a microcircuit (pg. 120, left column, 3rd paragraph) the method comprising: beginning random simulation (pg. 120, right paragraph, lines 4-13) of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for

beginning formal simulation (pg. 122, left column, lines 1-7) of a sequence of states of said microcircuit design; beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation (pg. 122, left column, second paragraph) states in a formal simulation model of said microcircuit design; monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 2: The method of Claim 1, wherein said random simulation model and said formal simulation model are the same (pg.121, right column, 6th paragraph).

Claim 3:The method of Claim 1, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 4: The method of Claim 1, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 5: The method of Claim 1, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 9: A method of verifying a design for a microcircuit (pg. 12, left column, 3rd paragraph), the method performed by a data processing system and comprising: beginning random simulation (pg. 120, right paragraph, lines 4-13) of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of states of said microcircuit design; beginning formal simulation (pg. 122, left column, lines 1-7) of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states (pg. 122, left column, second paragraph) in a formal simulation model of said microcircuit design; monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 10: The method of Claim 9, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 11: The method of Claim 9, wherein said simulating a sequence of formal simulation 10 states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 12: The method of Claim 9, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 13: The method of Claim 9, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 17: A data processing system for verifying a design for a microcircuit, the system comprising (pg. 124, right column, 3rd paragraph): a circuit configured for random simulation of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model (pg.120, right paragraph, lines 4-13) to obtain a sequence of random simulation states; a circuit configured for monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of states of said microcircuit design; a circuit configured for beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to

simulate a sequence of formal simulation states (pg. 122, left column, second paragraph) in a formal simulation model of said microcircuit design; a circuit configured for monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design; and a circuit configured for resuming said generation of said random input vector sequence for said random simulation mode' of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 18: The system of Claim 17, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 19: The system of Claim 17, wherein said simulating a sequence of formal simulation 15 states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 20: The system of Claim 17, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 21: The system of Claim 17, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 25: A computer program product comprising a computer usable medium having computer readable code embodied therein for verifying a design for a microcircuit, the computer program product comprising (pg. 120, right column, first paragraph): computer readable program code devices configured to cause a computer to effect random simulation of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; computer readable program code devices configured to cause a computer to effect monitoring of a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation (pg. 120, right paragraph, lines 4-13) of a sequence of states of said microcircuit design; computer readable program code devices configured to cause a computer to effect beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states in a formal simulation model of said microcircuit design; computer readable program code devices configured to cause a computer to effect monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design; and computer readable program code devices configured to cause a computer to effect resuming said generation of said random input vector sequence for

said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 26: The product of Claim 25, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 27: The product of Claim 25, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 28: The product of Claim 25, wherein said simulating a sequence of formal simulation 10 states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 29: The product of Claim 25, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim Rejections - 35 USC § 103

15. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

16. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 6-8, 14-16, 22-24,30-36 are rejected under 35 U.S.C. 103 (a) as unpatentable by Ho et al. ("Smart Simulation Using Collaborative Formal and Simulation Engines"; IEEE (November 2000)) in view of Harer ("Design and Maintenance Specification for CTG Reachability & Control Subsystems" February 2000).

Ho et al. teaches a simulation-based functional verification tool which provides automatic test generation and unreachability analysis (abstract: lines 1-5); but doesn't teach injecting a previously simulated process or input vector.

Harer teaches injecting a previously completed simulation process to obtain the best possible outcome for a predetermine goal.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Harer to modify Ho since it would be advantageous to rid the chip/microprocessor of all possible errors to negate product recalls to avoid decreases in profits.

Claim 6: The method of Claim 1, wherein said beginning of formal simulation is initiated by simulating in said formal simulation model (Ho: pg. 122, left column, 2nd paragraph, lines 1-4) a state of said microcircuit design previously simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9,instructions 4 and 5).

Claim 7: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4), further comprising proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg 9, instruction 8).

Claim 8: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4), wherein said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric (Ho: pg. 122, left column, 2nd paragraph, lines 1-4), and resuming said random simulation is continued

until a previously defined set of goal states of said microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 7-10).

Claim 14: The method of Claim 9, wherein said beginning of formal simulation (Ho: pg. 122, left column, 2nd paragraph) is initiated by simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9, instruction 5).

Claim 15: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), further comprising proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg. 9, instructions 6 and 7).

Claim 16: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), wherein said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric, and resuming said random simulation is continued until a previously defined set of goal states of said microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 6-8).

Claim 22: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), wherein said beginning of formal simulation is initiated by simulating in said formal simulation model a state of said microcircuit design previously simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9, instruction 4).

Claim 23: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), further comprising a circuit configured for proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg 9, instruction 8).

Claim 24: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), wherein said circuits are configured such that said process of monitoring said simulation coverage progress metric, beginning formal simulation, monitoring said formal coverage progress metric (Ho: pg. 122, left column, 2nd paragraph, lines 1-4), and resuming said random simulation is continued until a previously-defined set of goal states of said microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 7-10).

Claim 30: The product of Claim 25 (Hop. 120, right column, first paragraph), wherein said beginning of formal simulation is initiated by simulating in said formal simulation model a state of said microcircuit design previously simulated by inputting at least a portion of said random input vector sequence to said random simulation model (Harer: pg. 9, instructions 6 and 7).

Claim 31: The product of Claim 25 (Ho: pg. 120, right column, first paragraph), further comprising proving at least one of a set of previously-defined goal states of said microcircuit design unreachable (Harer: pg. 9, instructions 6-8).

Claim 32: The product of Claim 25 (Ho: pg. 120, right column, first paragraph), wherein said process of monitoring said simulation coverage progress metric, beginning formal

simulation, monitoring said formal coverage progress metric, and resuming said random simulation is continued until a previously defined set of goal states of said microcircuit design are simulated or proved unreachable (Harer: pg. 9, instructions 7-12).

Claim 33: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state (Harer: pg. 8, instructions 1-3); and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state.

Claim 34: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), wherein said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state (Harer: pg. 8, instructions 1-3); and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design arid said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state.

Claim 35: The system of Claim 17(Ho: pg. 12, left column, 3rd paragraph), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state (Harer: pg 8-9, instructions 1-12).

Claim 36: The product of Claim 25 (Ho: pg. 12, left column, 3rd paragraph), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state(Harer: pg 8-9, instructions 1-12).

Correspondence Information

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:30 am- 5:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

April 22, 2004

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER